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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SHAH, NILESH R	
ART UNIT	**PAPER NUMBER**
2195	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/926,468	KATAYAMA, YOSHIAKI	
	Examiner	Art Unit	
	Nilesh Shah	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 are presented for examination.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:
3. The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.
4. Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
    a. The following claim language is not clearly define:
        i. As per claims 1,2 10-11 line 2, it is unclear what OSs is? (i.e. the abbreviation of IS should be expanded?).
        ii. As per claim 1, line 9 , it is unclear if the execution occurs on the secondary OS; line 11, it is not clearly indicated where the first OS interrupt occurs? (i.e. it is the timer interrupt?). Claim 11 has similar problems.
    b. As per claim 2, line 3 and 19, it is unclear what no task means? (i.e. there has been no requests? There has been no interrupt? How do you know is there is no

task?), line 22, it is unclear how the one would determine whether there exists any tasks to be executed? Claim 10 has similar problems.

Allowable Subject Matter

5. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims

Claim Rejections - 35 USC § 103

6. Claims 1-2, 4- 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soloman (6,269,409) in view Townsley et al (5,623,677) (hereinafter Townsley).

7. As per claim 1, Soloman teaches the invention substantially as claimed including a method which employs a plurality of OSs whose execution is controlled by a processor, wherein said plurality of OSs include:

a primary OS for receiving a timer interrupt issued from a hardware timer after a predetermined time lapse (col. 5 lines 5-20; col. 6 lines 11-65; col.7 lines 1-36);

a secondary OS treated as a task to be executed by said primary OS (abstract; col. 2 lines 14 – 30; col. 3 lines 44-65; col. 4 lines 33-55; col.6 lines 11-65; col. 5 lines 5-20);

upon receiving said timer interrupt, determining with said primary OS whether there exists any task executed (col. 3 lines 44-65; col. 4 lines 33-55); and

when the primary OS determines there exists any task to be executed on said secondary OS, interrupting said secondary OS by issuing a secondary-OS interrupt from the priary OS to the secondary OS (col. 2 lines 14 – 30; col. 3 lines 44-65; col. 4 lines 33-55; col.6 lines 11-65; col. 5 lines 5-20).

9. Sekiguchi does not teach a power saving processor.

   Townsley teaches a power saving processor (col. 3 lines 10-24; col. 17 lines 62-67).

10. It would have been obvious to one skilled in the art at the time of the invention to combine the teachings of Soloman and Townsley because Townsley's method of power saving would improve Soloman's system by reducing power used when the processor is not being used.

11. As per claim 2, Soloman teaches which employs a plurality of OSs whose execution is controlled by a processor,

    operation of said processor being stopped when there exists no task to be executed on said plurality of OSs (col. 5 lines 5-20; col. 6 lines 11-65; col.7 lines 1-36);

    method controlling timer interrupt processing performed by a hardware timer which activates said processor after an arbitrary time lapse (col. 4 lines 33-55; col.6 lines 11-65; col. 5 lines 5-20);

    a primary OS for receiving a timer interrupt issued from said hardware timer and a secondary OS treated as a task to be executed by said primary OS (col. 2 lines 14 – 30; col. 3 lines 44-65; col. 4 lines 33-55; col.6 lines 11-65; col. 5 lines 5-20).

method comprises a primary-os process step performed by said primary OS, a secondary-os process step performed by said secondary OS, and a secondary-os interrupt step, said primary-os process step including, a step of detecting said timer interrupt (col. 5 lines 5-20; col. 6 lines 11-65; col.7 lines 1-36);

a first determination step of, upon receiving said timer interrupt, determining whether there exists any task to be executed and a processor stopping step of, when there is no task to be executed, stopping said processor (abstract; col. 2 lines 14 – 30; col. 3 lines 44-65; col. 4 lines 33-55; col.6 lines 11-65; col. 5 lines 5-20);

said secondary-os process step including:

a second determination step of determining whether there exists any task to be executed (; col. 3 lines 44-65; col. 4 lines 33-55; col.6 lines 11-65; col. 5 lines 5-20); and

a step of, when there is no task to be executed, handing over processing to said first determination step; said secondary – OS interrupt step including receciving a secondary OS interrupt from said primary OS (col. 3 lines 44-65; col. 4 lines 33-55; col.6 lines 11-65; col. 5 lines 5-20);

when said first determination step has determined that there exists any task to be executed on said secondary OS, interrupt processing on said secondary OS, and executes said second determination step at a predetermined time measured from said interrupt (col. 2 lines 14 – 30; col. 3 lines 44-65; col. 4 lines 33-55; col.6 lines 11-65; col. 5 lines 5-20);

Townsley teaches a power saving processor (col. 3 lines 10-24; col. 17 lines 62-67).

12. As per claim 4, Soloman teaches a method wherein said secondary-os interrupt step is executed by an alarm handler which interrupts said secondary OS after a specified time period (col. 2 lines 14 – 30; col. 3 lines 44-65; col. 4 lines 33-55; col.6 lines 11-65; col. 5 lines 5-20).

13. As per claim 5, Soloman teaches a method wherein said secondary-os interrupt step is executed by a high-priority task which is a task for interrupting said secondary OS and has a highest priority order among tasks to be executed by said primary OS (col. 5 lines 5-20; col. 6 lines 11-65; col.7 lines 1-36).

14. As per claim 6, Soloman teaches a method wherein said processor stopping step includes a step of determining whether time taken until said hardware timer issues a next timer interrupt is longer than a predetermined time, and if a measured time is longer than said predetermined time, said processor stopping step stops operation or said processor (col. 2 lines 14 – 30; col. 3 lines 44-65; col. 4 lines 33-55; col.6 lines 11-65; col. 5 lines 5-20).

15. As per claim 7, Soloman teaches a method wherein said primary-os process step further comprises steps of: when said hardware timer periodically performs timer interrupt processing at regular time intervals, determining whether timer interrupt processing is required again by a time at which a task is to be executed and if timer interrupt

processing is not required again, stopping said hardware timer(col. 3 lines 44-65; col. 4 lines 33-55; col.6 lines 11-65; col. 5 lines 5-20);

16. As per claim 8, Soloman teaches a method wherein said primary-os process step further comprises a step of:

detecting a timer interrupt issued by a long-periodic hardware timer which issues a timer interrupt at a time interval longer than that of said hardware timer (col. 3 lines 44-65; col. 4 lines 33-55; col.6 lines 11-65; col. 5 lines 5-20).

17. As per claim 9, Soloman teaches a method wherein said primary-os process step further comprises a step of:

detecting a timer interrupt issued by a time-of-day timer which measures a time of day as well as issuing a timer interrupt at a predetermined time or day (col. 5 lines 5-20; col. 6 lines 11-65; col.7 lines 1-36);

18. Claim 10 is rejected based on the same rejection as claim 2 above.

19. Claim 11 is rejected based on the same rejection as claims 1 and 2 above.

20. Claims 12-13 are rejected based on the same rejection as claim 8-9 above.

21. As per claim 14, Soloman teaches a method further comprising the step of: activating the secondary OS from a sleep mode in response to the secondary OS receiving the secondary -os interrupt issued from the primary OS (col. 3 lines 44-65; col. 4 lines 33-55; col.6 lines 11-65; col. 5 lines 5-20).

22. Claims 15-17 are rejected based on the same rejection as claim 14 above.

Response to Arguments

23. Applicant's arguments with respect to claims 1-17 filed on 7/1/05 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

24. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the

advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nilesh Shah whose telephone number is (571)272-3771. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571)272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nilesh Shah
Examiner
Art Unit 2195

NS
September 14, 2005

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